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EXAMINER	
VESPERMAN, WILLIAM C	
ART UNIT	**PAPER NUMBER**
2813	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/966,316	Applicant(s) MIS ET AL.	
	Examiner William C. Vesperman	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sh et with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28 and 62-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-5,8-28,62-72 and 74-76* is/are rejected.

7)☐ Claim(s) *6,7 and 73* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cit d (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This is in response to applicant's election/amendment of December 12, 2002.

Specification

2. The disclosure is objected to because of the following informalities. The Detailed Description, page 9, line 13 specifies layers 29a"-d" but should specify "27a"-d" with regards to Figure 1C and page 9, line 33 specifies Figure 3C but should specify Figure 3B with regards to items 51a" and 51d" instead.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 4, 8, 9, 13, 14, 62, 63, 66, 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rumsey et al. (US 2003/0000738 A1) in view of Huang (US 2002/0096764 A1).

Rumsey et al. (US 2003/0000738 A1) teaches (Figure 2, page 2, paragraph 0013 and 0014) a method of providing first and second input/output pads, attached to

substrate (10), comprising of bond pad(s) (18) with bonding wire attached (26) and contact pad(s) (19) with solder balls (30) attached.

Rumsey et al. (US 2003/0000738 A1) does not teach a shared metallurgy structure, over the input/output pads, adapted to receive solder and wire bonds.

Huang (US 2002/0096764 A1) teaches (Figure 7, page 2, paragraphs 0021-0024) a metallurgy structure (340a-340d) formed over contact pad (320) to receive a solder bump or gold bump (350). This structure includes a top layer (340d) comprising of copper which the applicant also has described in the Detailed Description and Figure 2C as suitable for wire bonding wire (26) or the bonding of the solder.bump (30).

Therefore, it would be obvious to one of ordinary skill in the art, to modify the method as taught by Rumsey et al. (US 2003/0000738 A1) to include a metallurgy structure (340a-340d) as taught by Huang (US 2002/0096764 A1) formed over the bond and contact pads in order to receive wire (26) or solder bumps (30).

One would be motivated to modify the method as taught by Rumsey et al. in order to include a metallurgy structure comprising of: under bump layers consisting of a titanium layer (340a) over the input/output pads in order to provide adhesion to the pads, followed by a first copper layer (340b) over the adhesion layer in order to provide better electrical or conductive performance, followed by a barrier layer or nickel-vanadium layer (340c) over the conductive layer to provide a barrier layer and finally a passivation layer or second copper layer (340d) over the barrier layer in order to provide a wetting layer and surface and solder bumps on the passivation layer to allow for solder bonding of a second substrate as taught by Huang (US 2002/0096764 A1).

5. Claims 2, 11, 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rumsey et al. (US 2003/0000738 A1) and Huang (US 2002/0096764 A1) as applied to claims 1, 3, and 62 respectively above, and further in view of Akram (US 2002/0182771 A1).

Rumsey et al. (US 2003/0000738 A1) and Huang (US 2002/0096764 A1) do not teach a method wherein the first and second metallurgy structures comprise a gold layer on the surface opposite the input/output pads.

Akram (US 2002/0182771 A1) teaches (Figure 7, page 5, paragraphs 0061-0062) a metallurgy structure referred to as a (UBM) under-bump metallurgy comprising of an adhesion layer, wetting layer and a gold protective layer on the surface opposite the input/output pads.

Therefore, it would be obvious to one of ordinary skill in the art, to modify the method as taught by Rumsey et al. (US 2003/0000738 A1) and Huang (US 2002/0096764 A1) to include a metallurgy structure as taught by Akram (US2002/0182771 A1) with a gold layer on the surface opposite the input/output pads.

One would be motivated to modify the method in order to obtain a nonoxidizable protective layer adjacent to the solder wetting layer as taught by Akram (US2002/0182771 A1).

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rumsey et al. (US 2003/0000738 A1) and Huang (US 2002/0096764 A1) as applied to claim 3 above.

Rumsey et al. (US 2003/0000738 A1) does not teach a method wherein providing the under-bump metallurgy layers comprises of providing a continuous under-bump metallurgy layer on the substrate and on the first and second input/output pads.

Huang (US 2002/0096764 A1) teaches (Figures 6, 7) providing a continuous under-bump metallurgy layer (340a) on the substrate and on the first and second input/output pads.

One would be motivated to modify the method to obtain a continuous under-bump metallurgy layer as taught by Huang (US 2002/0096764 A1) in order to reduce a mask step.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rumsey et al. (US 2003/0000738 A1) and Huang (US 2002/0096764 A1) as applied to 9 above, and further in view of Elenius (US 2001/0011764 A1).

Rumsey et al. (US 2003/0000738 A1) and Huang (US 2002/0096764 A1) do not teach a method wherein the barrier layers have a thickness in a range of 0.5 microns to 2.0 microns.

Elenius (US 2001/0011764 A1) teaches (Figure 2, page 4, paragraph 0034) that a UBM layer consisting of: titanium, nickel vanadium, copper and/or another suitable metal such as gold is approximately 2.0 microns thick. As a result, by dividing the approximate total thickness of 2.0 microns by the 3 and 4 layers previously discussed,

each layer or the barrier layer could be approximately in the range of 0.5 to 0.67 microns thick.

The selection barrier layers in a range of 0.50 microns and 2.0 microns. is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955) (the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980) (discovery of optimum value of result effective variable in a known process is obvious).

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rumsey et al. (US 2003/0000738 A1), Huang (US 2002/0096764 A1) and Akram (US 2002/0182771 A1) as applied to claim 11 above, and further in view of Elenius (US 2001/0011764 A1).

Rumsey et al. (US 2003/0000738 A1), Huang (US 2002/0096764 A1) and Akram (US 2002/0182771 A1) do not teach a method wherein the thickness of the gold layers is in a range of 0.50 microns and 2.0 microns.

Elenius (US 2001/0011764 A1) teaches (Figure 2, page 4, paragraph 0034) that a UBM layer consisting of: titanium, nickel vanadium, copper and/or another suitable metal such as gold is approximately 2.0 microns thick. As a result, by dividing the approximate total thickness of 2.0 microns by the 3 and 4 layers previously discussed, each layer or the gold layer could be approximately in the range of 0.5 to 0.67 microns thick.

The selection gold layers in a range of 0.50 microns and 2.0 microns. is obvious because it is a matter of determining optimum process condition by routine

experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955) (the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980) (discovery of optimum value of result effective variable in a known process is obvious).

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rumsey et al. (US 2003/0000738 A1) and Huang (US 2002/0096764 A1) as applied to claim 13 above, and further in view of Danziger et al. (US 6,221,682 B1).

Rumsey et al. (US 2003/0000738 A1) and Huang (US 2002/0096764 A1) do not teach a method wherein a first substrate is bonded to a second substrate via the solder structure.

Danziger et al. (US 6,221,682 B1) teaches (Figure 2) the bonding of die (14), to device (20) via the solder structure.

One would be motivated to modify the method as taught by Rumsey et al. (US 2003/0000738 A1) and Huang (US 2002/0096764 A1) to incorporate the solder bonding of the first substrate to the second substrate as taught by Danziger et al. (US 6,221,682 B1) in order to combine the memory or some other functions of the two substrates.

10. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rumsey et al. (US 2003/0000738 A1) in view of Huang (US 2002/0096764 A1) as applied to claim 1 above.

Rumsey et al. (US 2003/0000738 A1) does not teach a method wherein the electronic device comprises a protective insulating layer on the substrate and on

portions of the first and second input/output pads so that portions of the input/output pads are exposed through the protective insulating layer.

Huang (US 2002/0096764 A1) teaches (Figures 6, 7) the electronic device comprises a protective insulating layer (330) on the substrate (310) and on portions of the first and second input/output pads (320) so that portions of the input/output pads are exposed through the protective insulating layer.

One would be motivated to modify the method as by taught Rumsey et al. to provide a protective insulating layer on the substrate and on portions of the first and second input/output pads so that portions of the input/output pads are exposed through the protective insulating layer as taught by Huang (US 2002/0096764 A1) in order to insulate those portions of the contact pad not in contact with the under-bump layer (340b).

11. Claims 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (US 2002/0096764 A1) in view of Elenius (US 2001/0011764 A1).

Huang (US 2002/0096764 A1) teaches (Figure 7, paragraph 0021-0024) a method for providing a metallurgy structure (340) for an input/output pad (320) on the substrate (310), the method comprising: providing under bump layers on the input/output pad consisting of: titanium layer (340a) to provide an adhesion promoter, followed by a first copper layer (340b) to provide a better electrical or conductive performance, followed by a barrier layer on the under bump-layer consisting of nickel-vanadium layer (340c) to provide a barrier to migration layer and finally a passivation layer or second copper layer (340d) to provide a wetting layer and surface.

Huang does not teach a method wherein the barrier layer has a thickness in a range of 0.5 microns to 2.0 microns.

Elenius (US 2001/0011764 A1) teaches (Figure 2, page 4, paragraph 0034) that a UBM layer consisting of: titanium, nickel vanadium (barrier layer), copper and/or another suitable metal such as gold is approximately 2.0 microns thick. As a result, by dividing the approximate total thickness of 2.0 microns by the 3 and 4 layers previously discussed, each layer or the barrier layer could be approximately in the range of 0.5 to 0.67 microns thick.

The selection of the barrier layer in a range of 0.50 microns and 2.0 microns. is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955) (the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980) (discovery of optimum value of result variable in a known process is obvious).

12. Claims 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (US 2002/0096764 A1) in view of Akram (US 2002/0000738A1).

Huang (US 2002/0096764 A1) teaches (Figure 7, paragraph 0021-0024) a method for providing a metallurgy structure (340) for an input/output pad(s) (320) on the substrate (310), the method comprising: providing under bump layers on the input/output pad consisting of: titanium layer (340a) to provide adhesion, followed by a first copper layer (340b) to provide a better electrical or conductive performance, followed by a barrier layer on the under bump-layer consisting of nickel-vanadium layer

(340c) to provide a barrier to migration layer and finally a passivation layer or second copper layer (340d) on the barrier layer to provide a wetting layer and surface.

Huang does not teach a method wherein the metallurgy structure comprises a gold layer on the surface opposite the input/output pads

Akram (US 2002/0182771 A1) teaches (Figure 7, page 5, paragraphs 0061-0062) a metallurgy structure (UBM) under-bump metallurgy comprising of an adhesion layer, wetting layer and a gold protective layer on the surface opposite the input/output pads.

Therefore, it would be obvious to one of ordinary skill in the art, to modify the method as taught by Huang (US 2002/0096764 A1) to include a metallurgy structure with a gold layer on the surface opposite the input/output pad as taught by Akram (US 2002/0182771 A1).

One would be motivated to modify the method in order to obtain a nonoxidizable protective layer on the nickel barrier layer and adjacent to the solder wetting layer as taught by Akram (US2002/0182771 A1).

13. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (US 2002/0096764 A1) and Akram (US 2002/0000738A1) as applied to claim 22 above, and further in view of Elenius (US 2001/0011764 A1).

Huang (US 2002/0096764 A1) and Akram (US 2002/0000738A1) do not teach a method wherein the thickness of the gold layer is in a range of 0.05 to 2.0 microns.

Elenius (US 2001/0011764 A1) teaches (Figure 2, page 4, paragraph 0034) that a UBM layer consisting of: titanium, nickel vanadium, copper and/or another suitable

metal such as gold is approximately 2.0 microns thick. As a result, by dividing the approximate total thickness of 2.0 microns by the 3 and 4 layers previously discussed, each layer or the gold layer could be approximately in the range of 0.5 to 0.67 microns thick.

The selection gold layers in a range of 0.50 microns and 2.0 microns.
is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955) (the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

14. Claims 64 and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rumsey et al. (US 2003/0000738 A1) and Huang (US 2002/0096764 A1) as applied to claim 1 above, and further in view of Huang (US 2002/0096764 A1).

Rumsey et al. (US 2003/0000738 A1) does not teach reflowing the solder structure so that the passivation layer diffuses into the solder structure and that lead from the solder structure diffuses into the first barrier layer.

Huang (US 2002/0096764 A1) teaches (Figure 7, paragraph 0023-0029) that the solder bump material (containing lead) in contact with the copper passivation layer is reflowed.

Therefore, it would be obvious to one of ordinary skill in the art, to modify the method as taught by Rumsey et al. (US 2003/0000738 A1) and Huang (US 2002/0096764 A1) to include a reflow step as taught by Huang. Since the applicant has

specified in the Detailed Description and claim that the passivation layer can be copper, that the barrier layer can be nickel and the solder contains lead as taught by Huang (US 2002/0096764 A1), then it is inherent after the reflow step, that lead from the solder structure diffuses into the passivation layer and diffuses into portions of the first barrier layer.

One would be motivated to reflow the solder in order to improve the bond strength of the copper and nickel layers with regards to the solder layer and reduce possible voids in the structure.

15. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (US 2002/0096764 A1) as applied to 69, and further in view of Akram (US 2002/0000738A1).

Huang does not teach a method wherein the metallurgy structure comprises a gold layer on the surface opposite the input/output pads

Akram (US 2002/0182771 A1) teaches (Figure 7, page 5, paragraphs 0061-0062) a metallurgy structure (UBM) under-bump metallurgy comprising of an adhesion layer, wetting layer and a gold protective layer on the surface opposite the input/output pads.

Therefore, it would be obvious to one of ordinary skill in the art, to modify the method as taught by Huang (US 2002/0096764 A1) to include a metallurgy structure with a gold layer on the surface opposite the input/output pad as taught by Akram (US 2002/0182771 A1).

One would be motivated to modify the method in order to obtain a nonoxidizable protective layer on the nickel barrier layer and adjacent to the solder wetting layer as taught by Akram (US2002/0182771 A1). In addition, the passivation layer (340) on the input/output pads, being made of gold is adapted to receive solder or wirebonds as disclosed by the applicant (Figure 2C, and page 5 of the Detailed Description).

Claim Rejections - 35 USC § 102

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

17. Claims 17, 18, 19, 20, 24, 25, 26, 27, 28, 69, 70, 71, 72, 75, 76 are rejected under 35 U.S.C. 102(e) as being anticipated by or, in the alternative, under 103(e) as obvious over Huang (US 2002/0096764 A1).

In regards to claims 17, 18, 19, 20, 24, 25, 27, 28, 69, 70, 71, 72, 76 Huang (US 2002/0096764 A1) teaches (Figure 7, paragraph 0021-0024) a method for providing a metallurgy structure (340) for an input/output pad(s) on the substrate (310), the method comprising: providing under-bump layers on the input/output pad(s) consisting of: titanium layer (340a) to provide an adhesion promoter, followed by a first copper layer (340b) to provide a better electrical or conductive performance, followed by a barrier layer on the under bump-layer consisting of nickel-vanadium layer (340c) to provide a

barrier to migration layer and finally a passivation layer or second copper layer (340d) on the barrier layer to provide a wetting layer and surface. A solder structure (350) is on metallurgy structure(s) opposite the substrate and a protective insulating layer (330) is on the substrate (310) and on portions of the input/output pad(s) (320) so that portions of the input/output pad(s) are exposed through the protective insulating layer. In addition, the passivation layer (340) on the input/output pads, being made of copper is adapted to receive solder or wirebonds as disclosed by the applicant (Figure 2C, and page 5 of the Detailed Description).

In regards to claim 26, 75 Huang (US 2002/0096764 A1) teaches (Figure 7 and Summary of the Invention, paragraph 0012) that the semiconductor of the present invention can be directly mounted to an interconnection substrate by means of the attached solder bump electrodes.

Allowable Subject Matter

18. Claims 6, 7 and 73 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The following is a statement of reasons for the indication of allowable subject matter.

The prior art does not fairly teach or suggest that the method of providing the barrier layers comprise selectively electroplating the barrier layer on the under-bump

metallurgy layer and providing the passivation layers comprise selectively electroplating the passivation layer on the barrier layer. The barrier layer comprises a nickel layer free of lead and an alloy layer including nickel and lead between the nickel layer free of lead and the solder structure.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jao (US 6,415,974 B2) teaches a structure with solderbumps with improved coplanarity.

Chiang (US 2002/0086520) teaches a semiconductor device having a bump electrode.

Yung (US 5,162,257) teaches a solder bump fabrication method.

Ma (US 6,208,018 B1) teaches a piggyback multiple dice assembly.

Merrill et al. (US 5,886,393) teaches a bonding wire inductorfor use in an integrated circuit.

Mis (5,902,686) teaches methods for forming an inter-metallic region between a solder bump and a under-bump metallurgy region.

Kuo (US 2002/01978842 A1) teaches a solder bump process using a solder reservoir.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 703-305-1939. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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Art Unit 2813

February 4, 2003

CARL WHITEHEAD, JR
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800